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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,866	03/30/2004	Christopher J. Diorio	IMPJ-0027B	5628

49684 7590 07/16/2007

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
07/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,866	DIORIO ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-30,33-52,54,55 and 58-73* is/are rejected.

7)☒ Claim(s) *31,32,53,56,57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for continued examination filed 07 May 2007 has been received. The amended claims received 07 May 2007 are considered below.

Claim Objections

Claims 1, and 13 are objected to because of the following informalities:

With respect to claim 1, the recitation of "one of first or second" should be changed to -- one of a first and second --.

Claim 13 depends on cancelled claim 12.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Pascucci (USPN 5,854,762)

With respect to claim 1, Pascucci discloses in Fig. 2, a device comprising:

"a logic gate (latched inverters of 6) having an output node connected to the circuit (output of 6 is coupled to a circuit, i.e., 5, which is controlled by 6 via node 03,

i.e., UGVdis);

at least one nonvolatile memory element (M1 of 3), said at least one nonvolatile memory element configured to be programmed to a memory value capable of causing the output of said logic gate to settle to one of first or second predetermined states as a power-up or a reset signal is applied to the fuse (when the POR signal is applied to the fuse at node 16 as a low voltage signal, M5 will turn on to allow the value stored in M1 to be supplied to 6, thus controlling the logic value, i.e., high or low, of the output of 6), the first predetermined state of the output of the logic gate establishing a first configuration (the first predetermined state corresponds to when the voltage level DIS at the gate of M1 is too low, i.e., below the threshold of M1. At this point 6 is controlled to provide a low signal as UGVdis. Thus, "the circuit" 5 is configured to be turned on and to output a high UGV signal) the second predetermined state of the output of the logic gate establishing a second configuration (the second state is when DIS is at or above the threshold of M1, thus turning on M1 to pull DW of 6 low to activate UGVdis, therefore deactivating, i.e., "second configuration" of "the circuit" 5)."

With respect to claim 2, Pascucci discloses, that M1 is a floating a gate transistor wherein the amount of charge on said gate determines the memory value.

With respect to claims 4, Pascucci discloses, M1 is fabricated by a MOS process.

With respect to claims 5, Pascucci discloses, M1 is a floating gate transistor fabricated by a MOS process.

With respect to claims 6, Pascucci discloses, that M1 uses dielectric change to store information, since the control gate of M1 is capacitively coupled to the floating gate through a dielectric layer (see Col. 1 lines 34-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pascucci et al. (USPN 5,854,762) in view of Dugger et al. (USPAPN 2003/0183871).

With respect to claims 3 and 13, Pascucci et al. fails to disclose the floating gate nonvolatile memory element M1 having a first and second capacitor coupled to its floating gate. However, it is notoriously well-known in the art that floating gate transistors are composed of a first capacitor having a first plate in common with a floating gate of a floating gate transistor and a second "tunneling" capacitor having a plate in common with the floating. This is further evidenced, in Fig. 5 of Dugger et al., which discloses a nonvolatile memory transistor which has "a first capacitor having a first plate (572) in common with the floating gate (566) of said floating-gate transistor (520) " and "a second capacitor having a first plate (571) in common with the floating

gate (566) of said floating gate transistor (520) Dugger et al.'s capacitor allows for increased flexibility in programming the nonvolatile memory.

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the specific floating gate transistor 520 of Fig. 5 of Dugger et al. in place of the generic floating gate transistor of M1 of Pascucci et al. for the purpose of having a floating gate transistor with an increased flexibility in programming the transistor.

With respect to claims 7 and 8, the above combination discloses, changing the amount of charge on the floating gate using Fowler-Nordheim tunneling and hot-electron injection (see paragraph 0045).

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable Pascucci (USPN 5,854,762) in view of Madurawe (USPAPN 2005/0149896).

With respect to claims 7-11, Pascucci fails to disclose the floating gate transistor of M1 being programmed by bidirectional Fowler-Nordheim tunneling, Fowler-Nordheim tunneling, hot-electron injection, direct tunneling, and ultraviolet radiation exposure. However, it is notoriously well-known in the art that all of the recited programming are known programming procedures and a nonvolatile floating gate transistor can be programmed by any of the recited procedures of claims 7-11. This is further evidenced in lines 20-21 paragraph [010] of Madurawe, which discloses the choice of the above programming techniques are well-known in the art and chosen from user to user.

It would have been obvious to one of ordinary skill in the art to use any of the disclosed programming techniques as disclosed in paragraph [0010] of Madurawe to program the floating gate transistor M1 of Pascucci depending upon a desired application or a particular environment of use, the selection of a particular process of steps of programming the nonvolatile memory would have been performed to ensure an optimal performance of the circuit.

Claims 14-17, 19-21, 28-30, 33-38, 41-43, 51, 52, 54, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imodi (USPN 6,967,889) in view of Santin et al. (USPN 6,654,272)

With respect to claims 14 and 33, Imodi discloses, in Fig. 4, "a master-slave electronic fuse (circuit of Fig. 4), comprising:

a master fuse (201) having a nonvolatile memory element (201 is a Flash fuse i.e., nonvolatile memory) coupled between a reset node (node coupled to 411) of the master-slave electronic fuse and a first node of a master latch (201 is coupled to 411 via 403 and 409),

a slave latch (400) having a slave-latch input coupled to an output of the master latch (the gates of 412 and 414 of 400 are coupled to the output of 201 via 403, 409 and 411) and a slave-latch node configured to receive a slave-latch signal (the gates of 412 and 414 receive the slave latch signal, i.e., out of 411),

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal (READ_b) to the reset

node (201 settles to a programmed state or an erased state both before and after the application of READ_b), and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (When READ_b is low, 400 will latch the value of the programmed or erased output of 201) and wherein the first state to which the master latch is configured to settle is operative to configure the circuit to a corresponding first configuration and the second to which the master latch is configured to settle is operative to configure the circuit to a second corresponding second configuration (the output of 201 settles in a first and second thus causing the slave latch to also settle its output according to the first and second stage. Accordingly, the slave latch output changes the configuration of the circuit receiving the OUT signal for latch 400)."

Imodi fails to disclose the master fuse having a "master latch" and "a second nonvolatile memory element". Note that 201 of Imodi is merely a generic flash fuse. Santin et al. discloses in Fig. 1 a specific flash fuse composed of a master latch (120 with 122) and two nonvolatile memory elements (112 with 114).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the generic flash fuse 210 of Fig. 4 of Imodi with the specific flash fuse of Fig. 1 of Santin et al. for the purpose of providing a simply constructed specific flash fuse in place the generic flash fuse 210 of Imodi, which may be composed of any flash fuse circuit.

With respect to claim 15, the above combination discloses, that the state of the master latch composed of 120 and 122 of Santin et al. is controlled by the state of both nonvolatile memories (112 and 114).

With respect to claim 16, the above combination discloses, that the master latch operates effectively as cross coupled inverters.

With respect to claim 17, the above combination discloses, that 112 is a floating a gate transistor wherein the amount of charge on said gate determines the memory value.

With respect to claims 19 and 41, the above combination discloses, that 112 is fabricated by a MOS process.

With respect to claims 20 and 42, the above combination discloses, that 112 is a floating gate transistor fabricated by a MOS process.

With respect to claims 21 and 43, the above combination discloses, that 112 uses dielectric change to store information, since the control gate of 112 is capacitively coupled to the floating gate through a dielectric layer.

With respect to claim 28, the above combination discloses, that 128 is a "capacitive element" which is coupled to the output of the master latch of 120 and 122, since all electronic circuit elements inherently have an associated capacitance.

With respect to claims 29, 54 and 72, the above combination discloses, the charge on the floating gate of 112 and 113 dictates the programmed state of the nonvolatile memory, which in turn will be used to program master latch 120 with 122's output to complementary voltages on lines 138 and 136. Each programming state

corresponds to a high threshold voltage, i.e., writing stage, and a low threshold, i.e. erasing state, of the nonvolatile memories.

With respect to claims 30, 51 and 55, the above combination discloses, 128 is a "capacitive element" which is coupled to the output of the master latch of 120 and 122, since all electronic circuit elements inherently have an associated capacitance. Furthermore, 128 is also coupled between the output of the master latch and a fixed voltage source (i.e., one of the supply voltage and ground. The capacitive PMOS transistor of 128 is coupled to the supply voltage).

With respect to claim 34, the above combination discloses, the predetermined state is controlled by the programming/erasing of the first memory 112 of Santin et al.

With respect to claim 35, the above combination discloses, the predetermined state is controlled by the programming/erasing of the first memory 114 of Santin et al.

With respect to claims 36, the above combination discloses, the predetermined state of the master latch is affected by the memory value associated with 112 and 114 of Santin et al.

With respect to claim 37, the above combination discloses, that 112 and 113 of Santin et al. are both composed of a floating gate transistor and its programmed value is determined by the amount of charge present at its floating gate."

With respect to claim 38, the above combination discloses, that 112 and 113 of Santin et al. are both composed of a floating gate transistor and its programmed value is determined by the amount of charge present at its floating gate."

With respect to claim 52, the above combination discloses, the second output 138 of the master latch of Santin et al. is coupled to the capacitive NMOS transistor of 128 which is coupled to ground.

Claims 18; 27, 39, 40, 49, 50, 58-64, 67, 71, 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Imodi (USPN 6,967,889) and Santin et al. (USPN 6,654,272) as applied to claims 14-17, 19-21, 28-30, 33-38, 41-43, 51, 52, 54 and 55 in view of Dugger et al. (USPAPN 2003/0183871).

The above combination fails to disclose the floating gate nonvolatile memory elements 112 and 114 having a first and second capacitor coupled to its floating gate. However, it is notoriously well-known in the art that floating gate transistors a composed of a first capacitor having a first plate in common with a floating gate of a floating gate transistor and a second "tunneling" capacitor having a plate in common with the floating. This is further evidenced, in Fig. 5 of Dugger et al., which discloses a nonvolatile memory transistor which has "a first capacitor having a first plate (572) in common with the floating gate (566) of said floating-gate transistor (520) " and "a second capacitor having a first plate (571) in common with the floating gate (566) of said floating gate transistor (520). Dugger et al.'s capacitor allows for increased flexibility in programming the nonvolatile memory.

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the specific floating gate transistor 520 of Fig. 5 of Dugger et al. in place of the generic floating gate transistor of 112 and 114 of Santin et al. for the

purpose of having a floating gate transistor with an increased flexibility in programming the transistor.

With respect to claims 18, 27, 39, 40, 49 and 50, as can be seen above the above combination discloses, that each floating gate transistor of 112 and 114 of Santin et al. has a first capacitor having a first plate (572) in common with the floating gate (566) of said floating-gate transistor (520) " and "a second capacitor having a first plate (571) in common with the floating gate (566) of said floating gate transistor (520).

With respect to claims 58 and 73, the above combination is a circuit comprising:

a master fuse (201) having a logic gate element (flip-flop of Fig. 1 of Santin et al. as combined above) with a rest node (node coupled to 411) and a nonvolatile memory element comprising a MOSFET having a floating gate configured to receive charge by the way of hot-electron injection, and further comprising a tunnel capacitor sharing said floating gate as a capacitor plate which is configured to lose charge by way of tunneling (as modified above 112 and 114 of Santin et al. are replaced by the floating gate transistor of Fig. 5 of Dugger et al., which comprise a MOSFET having a floating gate 566, and receives and loses charge via hot-electron injection and tunneling capacitor 562 respectively, see paragraph 0045 of Dugger et al.); and

a slave latch (400) having a slave-latch input coupled to an output of the master fuse (the gates of 412 and 414 of 400 are coupled to the output of 201 via 403, 409 and 411) and a slave-latch node configured to receive a slave-latch signal (the gates of 412 and 414 receive the slave latch signal, i.e., out of 411),

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal (READ_b) to the reset node (201 settles to a programmed state or an erased state both before and after the application of READ_b), and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (When READ_b is low, 400 will latch the value of the programmed or erased output of 201) and wherein the first state to which the master latch is configured to settle is operative to configure the circuit to a corresponding first configuration and the second to which the master latch is configured to settle is operative to configure the circuit to a second corresponding second configuration (the output of 201 settles in a first and second thus causing the slave latch to also settle its output according to the first and second stage. Accordingly, the slave latch output changes the configuration of the circuit receiving the OUT signal for latch 400)."

With respect to claim 59, the above combination discloses, the predetermined state is controlled by the programming/erasing of the first memory 114 of Santin et al.

With respect to claim 60, the above combination discloses the predetermined state of the master latch is affected by the memory value associated with 112 and 114 of Santin et al.

With respect to claims 61 and 71, in the above combination, each floating gate transistor of 112 and 114 of Santin et al. has a first capacitor having a first plate (572) in common with the floating gate (566) of said floating-gate transistor (520) " and "a

second capacitor having a first plate (571) in common with the floating gate (566) of said floating gate transistor (520).

With respect to claim 62, the above combination discloses, that 112 is fabricated by a MOS process.

With respect to claim 63, the above combination discloses, that 112 is a floating gate transistor fabricated by a MOS process.

With respect to claim 64, the above combination discloses, that 112 uses dielectric change to store information, since the control gate of 112 is capacitively coupled to the floating gate through a dielectric layer.

With respect to claim 72, the above combination discloses, the charge on the floating gate of 112 and 113 dictates the programmed state of the nonvolatile memory, which in turn will be used to program master latch 120 with 122's output to complementary voltages on lines 138 and 136. Each programming state corresponds to a high threshold voltage, i.e., writing stage, and a low threshold, i.e. erasing state, of the nonvolatile memories.

Claims 22-27 and 39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable under the combination of Imodi (USPN 6,967,889) and Santin et al. (USPN 6,654,272) as applied to claims 14-17, 19-21, 28-30, 33-38, 41-43, 51, 52, 54 and 55 in further view of Madurawe (USPAPN 2005/0149896).

With respect to claims 22-27 and 39-43, the combination of Imodi and Santin et al. fails to disclose the floating gate transistors of 112, 114 of Santin et al. being

programmed by Fowler-Nordheim tunneling, direct tunneling, ultraviolet radiation exposure, hot-electron injection, hot-hole injection and bidirectional Fowler-Nordheim tunneling. However, it is notoriously well-known in the art that all of the recited programming are known programming procedures and a nonvolatile floating gate transistor can be programmed by any of the recited procedures of claims 22-27 and 39-43. This is further evidenced in lines 20-21 paragraph 0010 of Madurawe, which discloses the choice of the above programming techniques are well-known in the art and chosen from user to user.

It would have been obvious to one of ordinary skill in the art to use any of the disclosed programming techniques as disclosed in paragraph 0010 of Madurawe to program the floating gate transistor 112 and 114 of Santin et al. depending upon a desired application or a particular environment of use, the selection of a particular process of steps of programming the nonvolatile memory would have been performed to ensure an optimal performance of the circuit.

Claims 65-70 are rejected under 35 U.S.C. 103(a) as being unpatentable under the combination of Imodi (USPN 6,967,889), Santin et al. (USPN 6,654,272) and Dugger et al. (USPAPN 2003/0183871) as applied to claims 58-64, 71, and 72 in further view of Madurawe (USPAPN 2005/0149896).

With respect to claims 65-70, the combination of Imodi, Santin et al. and Dugger et al. fails to disclose the floating gate transistors of 112, 114 of Santin et al. being programmed by Fowler-Nordheim tunneling, direct tunneling, ultraviolet radiation

exposure, hot-electron injection, hot-hole injection and bidirectional Fowler-Nordheim tunneling. However, it is notoriously well-known in the art that all of the recited programming are known programming procedures and a nonvolatile floating gate transistor can be programmed by any of the recited procedures of claims 65-70. This is further evidenced in lines 20-21 paragraph 0010 of Madurawe, which discloses the choice of the above programming techniques are well-known in the art and chosen from user to user.

It would have been obvious to one of ordinary skill in the art to use any of the disclosed programming techniques as disclosed in paragraph 0010 of Madurawe to program the floating gate transistor 112 and 114 of Santin et al. depending upon a desired application or a particular environment of use, the selection of a particular process of steps of programming the nonvolatile memory would have been performed to ensure an optimal performance of the circuit.

Response to Arguments

Applicant's arguments with respect to claims 1-11, 13-30, 33-52, 54, 55 and 58-73 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 31, 32, 53, 56, and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth B. Wells/
Primary Examiner, Art Unit 2816

TH
July 11, 2007